

BEST AVAILABLE COPYIn the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) A method, comprising:

decoding an original first instruction into a complementary-predicated pair of instructions including a second predicate-positive instruction and a predicate-negative move instruction;

renaming both a first destination register of ~~said second~~ the predicate-positive instruction and a second destination register of ~~said~~ the predicate-negative move instruction to a same physical register; and

retiring either ~~said second~~ the predicate-positive instruction or ~~said~~ the predicate-negative move instruction responsive to a predicate value associated with both instructions.

2. (Currently Amended) The method of claim 1, wherein ~~said~~ the predicate-negative move instruction is responsive to a complement of ~~said~~ the predicate value.

3. (Currently Amended) The method of claim 1, wherein ~~said~~ the decoding includes sending a hint to a register renaming circuit that performs the renaming.

4. (Currently Amended) The method of claim 3, wherein ~~said~~ the sending includes sending ~~said~~ the hint via a trace cache.

5. (Currently Amended) The method of claim 1, further comprising sequencing ~~said second~~ the predicate-positive instruction and ~~said~~ the predicate-negative move instruction for out-of-order execution.

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6. (Currently Amended) The method of claim 5, further comprising squashing the predicate-negative move instruction when ~~said second~~ the predicate-positive instruction executes before ~~said~~ the predicate-negative move instruction and ~~said~~ the predicate value is true, ~~squashing said move instruction~~.
7. (Currently Amended) The method of claim 6, wherein ~~said~~ the squashing occurs before ~~said~~ the predicate-negative move instruction executes.
8. (Currently Amended) The method of claim 5, further comprising squashing the predicate-positive instruction [,] when ~~said~~ the predicate-negative move instruction executes before ~~said second~~ the predicate-positive instruction and ~~said~~ the predicate value is false, ~~squashing said second instruction~~.
9. (Currently Amended) The method of claim 8, wherein ~~said~~ the squashing occurs before ~~said second~~ the predicate-positive instruction executes.
10. (Currently Amended) A processor, comprising:
a decode circuit to decode an original first instruction into a ~~second~~ predicate-positive instruction and a predicate-negative move instruction;
a register renaming circuit to map a first destination register of ~~said second~~ the predicate-positive instruction to a physical register, and to map a second destination register of ~~said~~ the predicate-negative move instruction to the same said physical register; and
a retirement circuit to update ~~said~~ the physical register with a result of either ~~said second~~ the predicate-positive instruction or ~~said~~ the predicate-negative move instruction responsive to a predicate value associated with both instructions.

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11. (Currently Amended) The processor of claim 10, wherein said the predicate-negative move instruction is responsive to a complement of said the predicate value.
12. (Currently Amended) The processor of claim 10, wherein said the decode circuit sends a hint to said the register renaming circuit to permit said the mapping of said the first destination register and said the second destination register to said the same physical register.
13. (Currently Amended) The processor of claim 12, wherein said the hint is sent via a trace cache.
14. (Currently Amended) The processor of claim 10, further comprising a sequencer to permit out-of-order execution of said ~~second~~ the predicate-positive instruction and said the predicate-negative move instruction.
15. (Currently Amended) The processor of claim 14, wherein said the retirement circuit may squashes said the predicate-negative move instruction when said ~~second~~ the predicate-positive instruction executes before said the predicate-negative move instruction and said the predicate value is true.
16. (Currently Amended) The processor of claim 14, wherein said the retirement circuit may squashes said ~~second~~ the predicate-positive instruction when said the predicate-negative move instruction executes before said ~~second~~ the predicate-positive instruction and said the predicate value is false.
17. (Currently Amended) The processor of claim 14, further comprising execution units to execute said ~~second~~ the predicate-positive instruction and said the predicate-negative move instruction in parallel.

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18. (Currently Amended) A processor, comprising:

means for decoding an original first instruction into a complementary-predicated pair of instructions including a ~~second~~ predicate-positive instruction and a predicate-negative move instruction;

means for renaming both a first destination register of ~~said second~~ the predicate-positive instruction and a second destination register of ~~said~~ the predicate-negative move instruction to a same physical register; and

means for retiring either ~~said second~~ the predicate-positive instruction or ~~said~~ the predicate-negative move instruction responsive to a predicate value associated with both instructions.

19. (Currently Amended) The processor of claim 18, wherein ~~said~~ the predicate-negative move instruction is responsive to a complement of ~~said~~ the predicate value.

20. (Currently Amended) The processor of claim 18, wherein ~~said~~ the means for decoding includes means for sending a hint to a register renaming circuit.

21. (Currently Amended) The processor of claim 18, further comprising means for sequencing ~~said second~~ the predicate-positive instruction and ~~said~~ the predicate-negative move instruction for out-of-order execution.

22. (Currently Amended) The processor of claim 21, further comprising means for squashing ~~said~~ the predicate-negative move instruction when ~~said second~~ the predicate-positive instruction executes before ~~said~~ the predicate-negative move instruction and ~~said~~ the predicate value is true.

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23. (Currently Amended) The processor of claim 21, further comprising means for squashing ~~said second~~ the predicate-positive instruction when ~~said~~ the predicate-negative move instruction executes before ~~said second~~ the predicate-positive instruction and ~~said~~ the predicate value is false.
24. (Currently Amended) A system, comprising:
a processor, including:
a decode circuit to decode an original first instruction into a ~~second~~ predicate-positive instruction and a predicate-negative move instruction;[[,]]
a register renaming circuit to map a first destination register of ~~said second~~ the predicate-positive instruction to a physical register, and to map a second destination register of ~~said~~ the predicate-negative move instruction to the same ~~said~~ physical register;[[,]] and
a retirement circuit to update ~~said~~ the physical register with a result of either ~~said second~~ the predicate-positive instruction or ~~said~~ the predicate-negative move instruction responsive to a predicate value associated with both instructions;
a bus to couple ~~said~~ the processor to input/output devices; and
a communications device coupled to ~~said~~ the bus.
25. (Currently Amended) The system of claim 24, wherein ~~said~~ the predicate-negative move instruction is responsive to a complement of ~~said~~ the predicate value.
26. (Currently Amended) The system of claim 24, wherein ~~said~~ the decode circuit sends a hint to ~~said~~ the register renaming circuit to permit ~~said~~ the mapping of ~~said~~ the first destination register and ~~said~~ the second destination register to ~~said~~ the same physical register.

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27. (Currently Amended) The system of claim 24, further comprising a sequencer to permit out-of-order execution of ~~said second~~ the predicate-positive instruction and ~~said the~~ predicate-negative move instruction.
28. (Currently Amended) The system of claim 27, wherein ~~said the~~ retirement circuit may squashes ~~said the predicate-negative~~ move instruction when ~~said second the predicate-positive~~ instruction executes before ~~said the predicate-negative~~ move instruction and ~~said the~~ predicate value is true.
29. (Currently Amended) The system of claim 27, wherein ~~said the~~ retirement circuit may squashes ~~said second the predicate-positive~~ instruction when ~~said the predicate-negative~~ move instruction executes before ~~said second the predicate-positive~~ instruction and ~~said the~~ predicate value is false.